Amendments to the Claims

This listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims

1. -17. (canceled)

18. – 20. (withdrawn)

21. – 25. (canceled)

26. – 28. (withdrawn)

29. (currently amended): A thin film transistor (TFT), comprising:

a gate electrode with an island shape formed on a substrate;

an insulating layer covering the gate electrode;

a semiconductor layer with an island shape formed on the insulating layer, and positioned directly above the gate electrode;

a source doped silicon layer and a drain doped silicon layer formed on the semiconductor layer, a channel being defined between the source doped silicon layer and the drain doped silicon layer to expose the semiconductor layer therein;

first and second sacrifice layers with island shapes respectively formed on the source doped silicon layer and drain doped silicon layer and formed over the semiconductor layer ~~in their entirety~~, the first and the second sacrifice layers being spaced apart by the channel and further separate from the insulating layer in their entirety, wherein an entire bottom of the first and second sacrifice layers is higher than a top of the semiconductor layer ;

a source electrode formed above the first sacrifice layer and the source dope silicon layer; and

a drain electrode formed above the second sacrifice layer and the drain doped silicon layer.

30. (withdrawn)

31. (original) The TFT in claim 29, further comprising a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

32. (original) The TFT in claim 29, further comprising:

a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and

a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

33. (currently amended) A thin film transistor (TFT), comprising:

a gate electrode with an island shape formed on a substrate;

an insulating layer covering the gate electrode;

a semiconductor layer with an island shape formed on the insulating layer, and positioned above the gate electrode;

first and second sacrifice layers with island shapes formed over and in direct contact with the semiconductor layer in their entirety, and a channel being defined between the first and second sacrifice layers so as to expose the semiconductor layer;

a source doped silicon layer and a drain doped silicon layer formed above the first sacrifice layer, second sacrifice layer, and the semiconductor layer, the source doped silicon layer and the drain doped silicon layer being spaced apart by the channel, wherein the source doped silicon layer and the drain doped silicon layer are in contact with the semiconductor layer; and

a source electrode and a drain electrode respectively formed on the source doped silicon layer and the drain doped silicon layer.

34. (withdrawn)

35. (original) The TFT in claim 33, further comprising a passivation layer covering the source electrode, the drain electrode, and the channel, and the TFT is used in an in-plane-switch (IPS) type LCD.

36. (original) The TFT in claim 33 further comprising:

a passivation layer covering the TFT on the substrate, and having a hole above the drain electrode; and

a transparent conductive layer formed above the drain electrode and electrically connected to the drain electrode via the hole.

37.- 38. (withdrawn)

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